DS04-27801-1E

ASSP For Power Management Applications (Mobile Phones)

Power Management IC for GSM Mobile Phone

MB3891

■ DESCRIPTION

MB3891 is intended to be used in future GSM-phones, Dual Band phones and Dual Mode phones. It contains all the necessary functions to support all Digital, Analog and RF blocks in these phones. A Charge-pump including a Logic Level Translation circuit is built in to support SIM-card (SmartCard) of both 3 and 5 Volt technology. The circuit contains a charger for a rechargeable Lithium coin cell of a Real Time Clock.

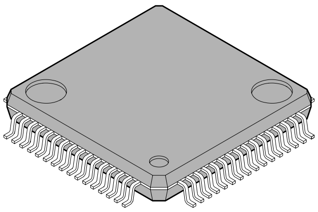
A complex control circuit is built in to generate main reset and to turn on and off the different LDO's.

■ FEATURES

- Supply voltage range : 3 V to 5.5 V
- Low power consumption current during standby : 400 μA (MAX)
- 6-channel low-saturation voltage type series regulator : 2.1 V/2 channels, 2.8 V/3 channels, 2.5 V/2.8 V switch
- Error prevention function during Low voltage
- Power on reset function
- 3 V/5 V SW for SIM-Card
- SIM interface function
- Backflow prevention function for Battery-Backup
- Temperature prevention function

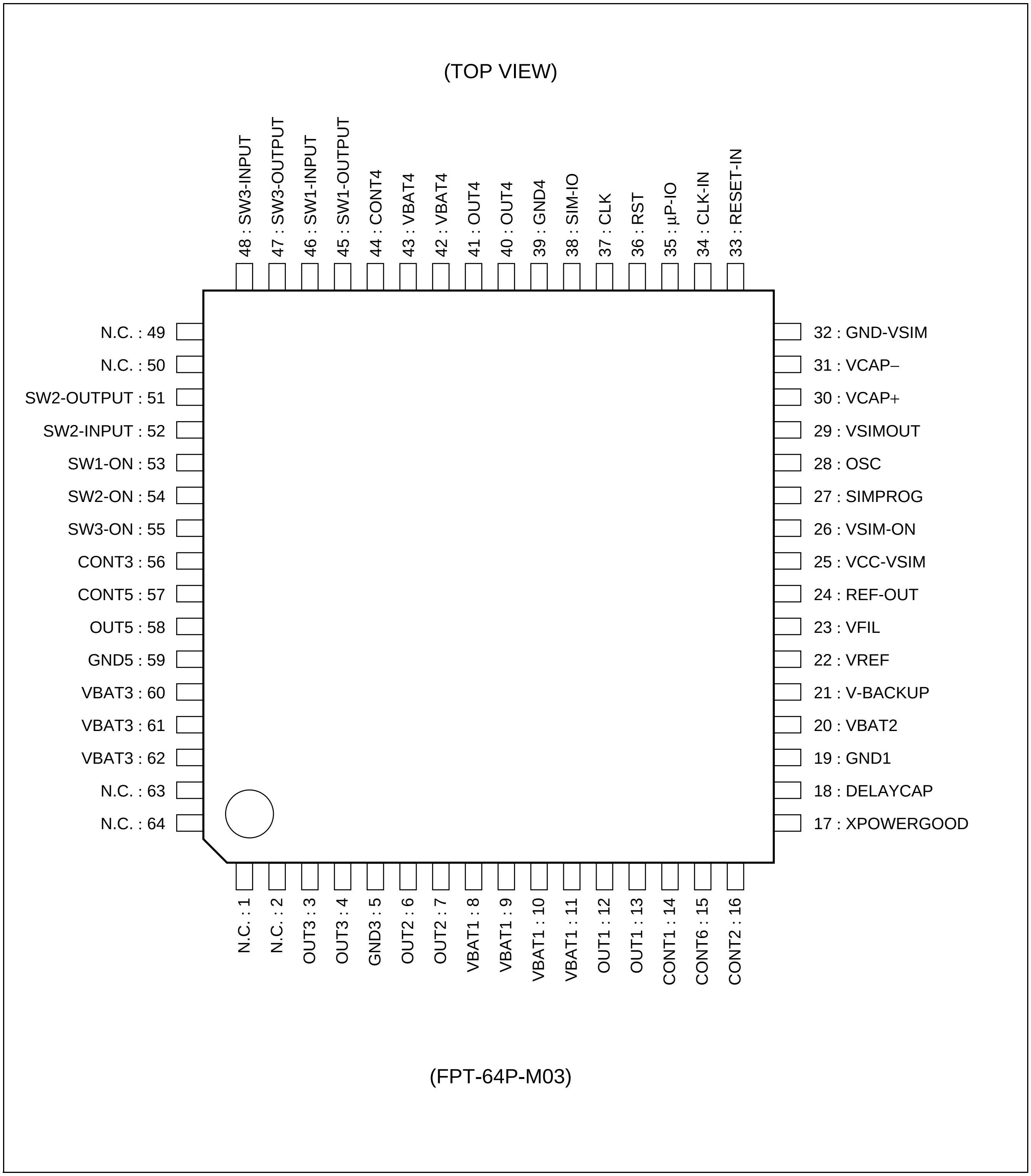
■ PACKAGE

64-pin plastic LQFP



(FPT-64P-M03)

■ PIN ASSIGNMENT



■ PIN DESCRIPTION

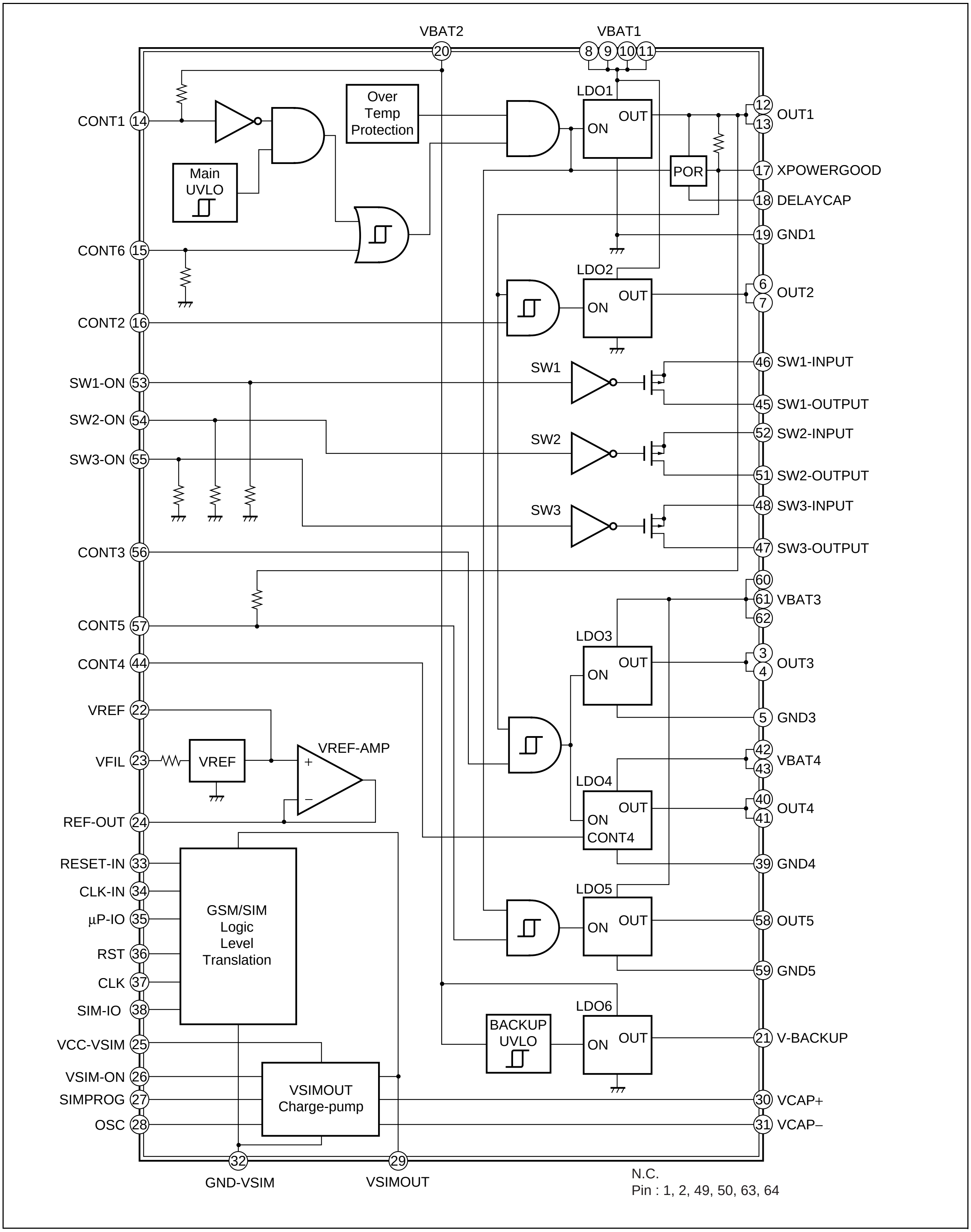
Pin No.	Symbol	I/O	Descriptions
1, 2	N.C.	—	Non connection.
3, 4	OUT3	O	LDO3 output pin.
5	GND3	—	LDO3 ground pin.
6, 7	OUT2	O	LDO2 output pin.
8, 9, 10, 11	VBAT1	—	Battery voltage input pin for LDO1 and LDO2.
12, 13	OUT1	O	LDO1 output pin.
14	CONT1	I	Power on input from keypad (Active low, Pulled up to VBAT2).
15	CONT6	I	“CONT6” input from digital system µP (Active high).
16	CONT2	I	External accessory supply voltage Enable (Active high).
17	XPOWERGOOD	O	Generates the main reset. (Active low, when OUT1 is out of regulation).
18	DELAYCAP	—	Timing capacitor for XPOWERGOOD delay.
19	GND1	—	LDO1, LDO2, V-BACKUP, Reference and System ground pin.
20	VBAT2	—	Battery voltage input pin for both UVLO’s, Reference and V-BACKUP LDO.
21	V-BACKUP	O	Supply voltage for Charger for rechargeable Lithium coin cell.
22	VREF	O	Supply voltage for Reference.
23	VFIL	O	Reference voltage Filter.
24	REF-OUT	O	Reference output voltage (Present when BACKUP UVLO is high).
25	VCC-VSIM	—	Input voltage for charge pump. (Supplied by VBAT1).
26	VSIM-ON	I	VSIM supply Enable (Active high).
27	SIMPROG	I	VSIM programming: Low = 3 V SIM, High = 5 V SIM.
28	OSC	—	Oscillator output pin.
29	VSIMOUT	O	Supply voltage for 3 or 5 V SIM-Card (SmartCard).
30	VCAP+	—	Positive side of boost capacitor.
31	VCAP–	—	Negative side of boost capacitor.
32	GND-VSIM	—	3 or 5 V SIM-Card (SmartCard) ground pin.
33	RESET-IN	I	Non level shifted SIM reset (µP side).
34	CLK-IN	I	Non level shifted clock (µP side).
35	µP-IO	I/O	Non level shifted bi-directional data input/output (µP side).
36	RST	O	Level shifted SIM reset (SmartCard side).
37	CLK	O	Level shifted SIM clock (SmartCard side).
38	SIM-IO	I/O	Level shifted bi-directional SIM data input/output (SmartCard side).
39	GND4	—	LDO4 ground pin.
40, 41	OUT4	O	LDO4 output pin.

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Pin No.	Symbol	I/O	Descriptions
42, 43	VBAT4	—	Supply voltage for LDO4.
44	CONT4	I	OUT4 output voltage selection (“L”=2.8 V,“H”=2.5 V).
45	SW1-OUTPUT	O	Output of general purpose switch number 1 (Drain).
46	SW1-INPUT	I	Input of general purpose switch number 1 (Source).
47	SW3-OUTPUT	O	Output of general purpose switch number 3 (Drain).
48	SW3-INPUT	I	Input of general purpose switch number 3 (Source).
49, 50	N.C.	—	Non connection.
51	SW2-OUTPUT	O	Output of general purpose switch number 2 (Drain).
52	SW2-INPUT	I	Input of general purpose switch number 2 (Source).
53	SW1-ON	I	General purpose switch number 1 Enable (Active high).
54	SW2-ON	I	General purpose switch number 2 Enable (Active high).
55	SW3-ON	I	General purpose switch number 3 Enable (Active high).
56	CONT3	I	OUT3 and OUT4 supply voltage Enable (Active high).
57	CONT5	I	OUT5 supply voltage Enable (Active high).
58	OUT5	O	Output terminal of LDO5.
59	GND5	—	LDO5 ground pin.
60, 61, 62	VBAT3	—	Supply voltage for LDO and LDO5.
63, 64	N.C.	—	Non connection.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating		Unit
			Min.	Max.	
Power supply voltage	VBAT	—	–0.3	7	V
	VCC-VSIM	—	–0.3	7	V
LDO regulator	I_O	OUT1 pin	—	120	mA
	I_O	OUT2 pin	—	50	mA
	I_O	OUT3 pin	—	100	mA
	I_O	OUT4 pin	—	100	mA
	I_O	OUT5 pin	—	50	mA
VSIMOUT chargepump	I_O	VSIMOUT pin	—	10	mA
Power dissipation	P_D	Ta ≤ +25 °C	—	800*	mW
Storage temperature	Tstg	—	–55	+125	°C

* : The packages are mounted on the dual-sided epoxy board(10 cm × 10 cm)

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Power supply voltage	VBAT	—	3.0	3.6	5.5	V
	VCC-VSIM	—	3.0	3.6	5.5	V
LDO capacitor guarantee value	C_O	OUT1 to OUT5, V-BACKUP pin	0.8	1.0	—	µF
REF-OUT capacitor guarantee value	C_O	REF-OUT pin	—	0.027	—	µF
VSIMOUT capacitor guarantee value	C_O	VSIMOUT pin	—	10	—	µF
Operating ambient temperature	Ta	—	–20	+25	+85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(Ta = +25 °C, VBAT1 to VBAT4 = VCC-VSIM = 3.6 V)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
General	Shutdown supply current	I_{BAT1}	8, 9, 10, 11, 20, 42, 43, 60, 61, 62	UVLO = “L”, BACKUP UVLO = “L”	—	—	80	µA
		I_{BAT2}	8, 9, 10, 11, 20, 42, 43, 60, 61, 62	UVLO = “L”, BACKUP UVLO = “H”	—	—	160	µA
	Standby supply current	I_{BAT3}	8, 9, 10, 11, 20, 42, 43, 60, 61, 62	All circuit’s = On (No load)	—	—	400	µA
	Operating ground current	I_{GND}	4, 5, 19, 32, 59	All circuit’s -VSIM = On Max. load on all regulators	—	—	10	mA
	UVLO threshold voltage	V_{THH}	8, 9, 10, 11, 20, 42, 43, 60, 61, 62	OUT1 = ON	2.980	3.080	3.180	V
		V_{THL}	8, 9, 10, 11, 20, 42, 43, 60, 61, 62	OUT1 = OFF	2.780	2.880	2.980	V
	BACKUP UVLO threshold voltage	V_{THH}	8, 9, 10, 11, 20, 42, 43, 60, 61, 62	V-BACKUP = ON	2.980	3.080	3.180	V
		V_{THL}	8, 9, 10, 11, 20, 42, 43, 60, 61, 62	V-BACKUP = OFF	2.580	2.680	2.780	V
	Input voltage	V_{IH}	16, 56, 57	—	0.7 × OUT1	—	OUT1	V
		V_{IL}	16, 56, 57	—	0	—	0.3 × OUT1	V
		V_{IH}	14, 15, 44	—	0.7 × VBAT	—	VBAT	V
		V_{IL}	14, 15, 44	—	0	—	0.3 × VBAT	V
		V_{IH}	26, 27	—	0.7 × VCC-VSIM	—	VCC-VSIM	V
		V_{IL}	26, 27	—	0	—	0.3 × VCC-VSIM	V
	Pull-up resistor	R_{PU}	17	—	—	15*	—	kΩ
		R_{PU}	14, 57	—	—	200*	—	kΩ
	Pull-down resistor	R_{PD}	15, 53, 54, 55	—	—	200*	—	kΩ

* : Standard design value

(Continued)

(Ta = +25 °C, VBAT1 to VBAT4 = VCC-VSIM = 3.6 V)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
LDO1 (OUT1)	Output voltage	V_O	12, 13	–50 μA > OUT1 > –120 mA	2.000	2.100	2.200	V
	Line regulation	Line	12, 13	3.1 V < VBAT1 < 5.5 V	—	—	10	mV
	Load reguration	Load	12, 13	–50 μA > OUT1 > –120 mA	—	—	30	mV
	Ripple rejection ΔVBAT1/ΔOUT1	R.R	12, 13	f = 217 Hz	45	—	—	dB
	Dropout voltage	V_{DO}	12, 13	OUT1 = –120 mA	—	—	500	mV
	GND current at low load	I_{GND}	19	OUT1 > –1 mA	—	—	30	μA
	GND current at max. load	I_{GND}	19	OUT1 = –120 mA	—	—	2	mA
	Output noise volt. (RMS)	V_{NOVL}	12, 13	f = 10 Hz to 1 MHz, OUT1 = 1 μF	—	—	500	μV
XPOWER-GOOD (RESET)	Output voltage	V_{OH}	17	—	0.8 × OUT1	—	OUT1	V
		V_{OL}	17	—	0	—	0.1 × OUT1	V
	Hold time	T_{XPG}	17	DELAYCAP = 0.033 μF	10	25	40	ms
LDO2 (OUT2)	Output voltage	V_O	6, 7	–50 μA > OUT2 > –50 mA	2.700	2.800	2.900	V
	Line regulation	Line	6, 7	3.1 V < VBAT1 < 5.5 V	—	—	10	mV
	Load regulation	Load	6, 7	–50 μA > OUT2 > –50 mA	—	—	30	mV
	Ripple rejection ΔVBAT1/ΔOUT2	R.R	6, 7	f = 217 Hz	45	—	—	dB
	Dropout voltage	V_{DO}	6, 7	OUT2 = –50 mA	—	—	250	mV
	GND current at low load	I_{GND}	19	OUT2 > –1 mA	—	—	30	μA
	GND current at max. load	I_{GND}	19	OUT2 = –50 mA	—	—	1	mA
	Output noise volt. (RMS)	V_{NOVL}	6, 7	f = 10 Hz to 1 MHz, OUT2 = 1 μF	—	—	350	μV
General purpose switches	Input/Output resistance	R_{SW1}	45, 46	SW1-INPUT = 2.8 V (Gate/Source = 2.8 V)	—	—	4.0	Ω
		R_{SW2}	51, 52	SW2-INPUT = 2.8 V (Gate/Source = 2.8 V)	—	—	7.0	Ω
		R_{SW3}	47, 48	SW3-INPUT = 2.8 V (Gate/Source = 2.8 V)	—	—	7.0	Ω

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(Ta = +25 °C, VBAT1 to VBAT4 = VCC-VSIM = 3.6 V)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
LDO3 (OUT3)	Output voltage	V_O	3, 4	–50 µA > OUT3 > –100 mA	2.700	2.800	2.900	V
	Line regulation	Line	3, 4	3.1 V < VBAT3 < 5.5 V	—	—	10	mV
	Load regulation	Load	3, 4	–50 µA > OUT3 > –100 mA	—	—	30	mV
	Ripple rejection ΔVBAT3/ΔOUT3	R.R	3, 4	f = 217 Hz	45	—	—	dB
	Dropout voltage	V_{DO}	3, 4	OUT3 = –100 mA	—	—	250	mV
	GND current at low load	I_{GND}	5	OUT3 > –1 mA	—	—	30	µA
	GND current at max. load	I_{GND}	5	OUT3 = –100 mA	—	—	2	mA
	Output noise volt. (RMS)	V_{NOVL}	3, 4	f = 10 Hz to 1 MHz, OUT3 = 1 µF	—	—	350	µV
LDO4 (OUT4)	Output voltage	V_O	40, 41	–50 µA > OUT4 > –100 mA, CONT4 = “L”	2.700	2.800	2.900	V
		V_O	40, 41	–50 µA > OUT4 > –100 mA, CONT4 = “H”	2.400	2.500	2.600	V
	Line regulation	Line	40, 41	3.1 V < VBAT4 < 5.5 V	—	—	10	mV
	Load regulation	Load	40, 41	–50 µA > OUT4 > –100 mA	—	—	30	mV
	Ripple rejection ΔVBAT4 - OUT4/ΔOUT4	R.R	40, 41	f = 217 Hz	45	—	—	dB
	Dropout voltage	V_{DO}	40, 41	OUT4 = –100 mA	—	—	250	mV
	GND current at low load	I_{GND}	39	OUT4 > –1 mA	—	—	30	µA
	GND current at max. load	I_{GND}	39	OUT4 = –100 mA	—	—	2	mA
	Output noise volt. (RMS)	V_{NOVL}	40, 41	f = 10 Hz to 1 MHz, OUT4 = 1 µF	—	—	500	µV
LDO5 (OUT5)	Output voltage	V_O	58	–50 µA > OUT5 > –50 mA	2.700	2.800	2.900	V
	Line regulation	Line	58	3.1 V < VBAT3 < 5.5 V	—	—	10	mV
	Load regulation	Load	58	–50 µA > OUT5 > –50 mA	—	—	30	mV
	Ripple rejection ΔVBAT3/ΔOUT5	R.R	58	f = 217 Hz	45	—	—	dB
	Dropout voltage	V_{DO}	58	OUT5 = –50 mA	—	—	250	mV
	GND current at low load	I_{GND}	59	OUT5 > –500 µA	—	—	20	µA
	GND current at max. load	I_{GND}	59	OUT5 = –50 mA	—	—	1	mA
	Output noise volt. (RMS)	V_{NOVL}	58	f = 10 Hz to 1 MHz, OUT5 = 1 µF	—	—	350	µV

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(Ta = +25 °C, VBAT1 to VBAT4 = VCC-VSIM = 3.6 V)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
LDO6 (V-BACKUP)	Output voltage	V_O	21	–10 µA > V-BACKUP > –250 µA	2.000	2.100	2.200	V
	Line regulation	Line	21	3.1 V < VBAT2 < 5.5 V	—	—	10	mV
	Load regulation	Load	21	–10 µA > V-BACKUP > –250 µA	—	—	30	mV
	Ripple rejection ΔVBAT2/ ΔV-BACKUP	R.R	21	f = 217 Hz	25	—	—	dB
	GND current at low load	I_{GND}	19	V-BACKUP > –10 µA	—	—	10	µA
	GND current at max. load	I_{GND}	19	V-BACKUP = –250 µA	—	—	50	µA
	Output noise volt. (RMS)	V_{NOVL}	21	f = 10 Hz to 1 MHz, V-BACKUP = 1 µF	—	—	500	µV
	Reverse current	I_{RC}	21	VBAT2 = 0 V, V-BACKUP = 3.0 V	—	—	100	nA
REF-OUT	Output voltage	V_O	24	0 µA > REF-OUT > –50 µA	1.200	1.225	1.250	V
	Line regulation	Line	24	3.1 V < VBAT2 < 5.5 V	—	—	10	mV
	Load regulation	Load	24	0 µA > REF-OUT > –50 µA	—	—	6	mV
	Ripple rejection ΔVBAT2/ ΔREF-OUT	R.R	24	f = 217 Hz	50	—	—	dB
	Output noise volt. (RMS)	V_{NOVL}	24	f = 10 Hz to 1 MHz, REF-OUT = 27 nF	—	—	250	µV
VSIMOUT chargepump	Output voltage	V_O	29	–50 µA > VSIMOUT > –10 mA, SIMPROG = “H”	4.600	5.000	5.400	V
		V_O	29	–50 µA > VSIMOUT > –10 mA, SIMPROG = “L”	2.760	3.000	3.240	V
	Line regulation	Line	29	3.1 V < VCC-VSIM < 5.5 V	—	—	50	mV
	Load regulation	Load	29	–50 µA > VSIMOUT > –10 mA	—	—	100	mV

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(Ta = +25 °C, VBAT1 to VBAT4 = VCC-VSIM = 3.6 V)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
VSIMOUT chargepump	Ripple rejection ΔVCC-VSIM/ ΔVSIMOUT	R.R	29	f = 217 Hz	30	—	—	dB
	Output current	I_O	29	3.1 V < VCC-VSIM < 5.5 V, VSIMOUT = 5 V	10	—	—	mA
		I_O	29	3.1 V < VCC-VSIM < 5.5 V, VSIMOUT = 3 V	6	—	—	mA
	GND current at no load	I_{GND}	32	VSIMOUT > –50 µA	—	—	100	µA
	Efficiency at max. load	η	25, 29	VSIMOUT = –10 mA, VSIMOUT = 5 V	85	—	—	%
	Output ripple voltage	V_{RP}	29	f = 10 Hz to 1 MHz, VSIMOUT = 10 µF	—	—	100	mV_{PP}
	Shutdown supply current	I_{LDO}	25	VSIM-ON = “L”	—	—	100	nA
GSM/SIM logic level translation µp interface	Input voltage	V_{IH}	33, 34, 35	—	0.7 × OUT1	—	OUT1	V
		V_{IL}	33, 34, 35	—	0	—	0.3 × OUT1	V
	Output voltage	V_{OH}	35	µP-IO (max.) = –20 µA	0.8 × OUT1	—	OUT1	V
		V_{OL}	35	µP-IO (max.) = 1 mA	0	—	0.2 × OUT1	V

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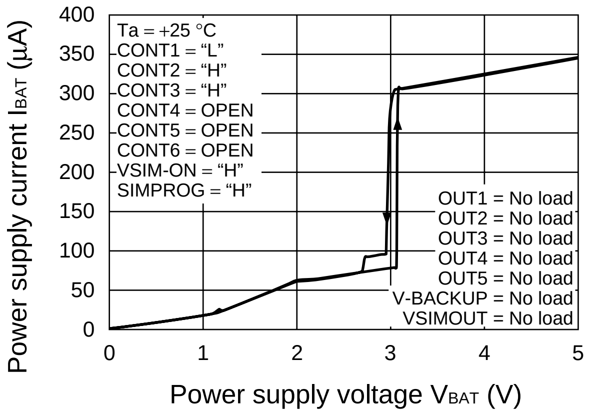
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(Ta = +25 °C, VBAT1 to VBAT4 = VCC-VSIM = 3.6 V)

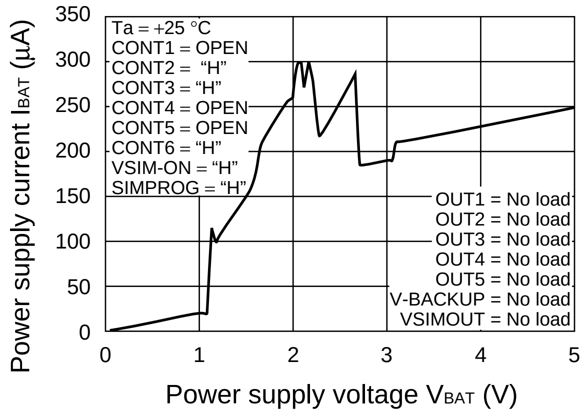
Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
SIM interface 5 V (SIMPROG = H)	Output voltage	V_{OH}	36	RST (max.) = –20 µA	VSIMOUT – 0.7	—	VSIMOUT	V
		V_{OL}	36	RST (max.) = 200 µA	0	—	0.6	V
	Rise time	T_R	36	RESET-IN = RST = 30 pF	—	—	400	µs
	Fall time	T_F	36	RESET-IN = RST = 30 pF	—	—	400	µs
	Output voltage	V_{OH}	37	CLK (max.) = –20 µA	0.7 × VSIMOUT	—	VSIMOUT	V
		V_{OL}	37	CLK (max.) = 200 µA	0	—	0.5	V
	Rise time	T_R	37	CLK-IN = CLK = 30 pF	—	—	27	ns
	Fall time	T_F	37	CLK-IN = CLK = 30 pF	—	—	27	ns
	Output voltage	V_{OH}	38	SIM-IO (max.) = –20 µA	3.8	—	VSIMOUT	V
		V_{OL}	38	SIM-IO (max.) = 1 mA	0	—	0.4	V
	Input voltage	V_{IH}	38	—	0.7 × VSIMOUT	—	VSIMOUT	V
		V_{IL}	38	—	0	—	0.8	V
	Rise time	T_R	38	SIM-IO = 30 pF	—	—	1	µs
	Fall time	T_F	38	SIM-IO = 30 pF	—	—	1	µs
SIM interface 3 V (SIMPROG = L)	Output voltage	V_{OH}	36	RST (max.) = –20 µA	0.8 × VSIMOUT	—	VSIMOUT	V
		V_{OL}	36	RST (max.) = 200 µA	0	—	0.2 × VSIMOUT	V
	Rise time	T_R	36	RESET-IN = RST = 30 pF	—	—	400	µs
	Fall time	T_F	36	RESET-IN = RST = 30 pF	—	—	400	µs
	Output voltage	V_{OH}	37	CLK (max.) = –20 µA	0.7 × VSIMOUT	—	VSIMOUT	V
		V_{OL}	37	CLK (max.) = 200 µA	0	—	0.2 × VSIMOUT	V
	Rise time	T_R	37	CLK-IN = CLK = 30 pF	—	—	50	ns
	Fall time	T_F	37	CLK-IN = CLK = 30 pF	—	—	50	ns
	Output voltage	V_{OH}	38	SIM-IO (max.) = –20 µA	0.7 × VSIMOUT	—	VSIMOUT	V
		V_{OL}	38	SIM-IO (max.) = 1 mA	0	—	0.4	V
	Input voltage	V_{IH}	38	—	0.7 × VSIMOUT	—	VSIMOUT	V
		V_{IL}	38	—	0	—	0.2 × VSIMOUT	V
	Rise time	T_R	38	SIM-IO = 30 pF	—	—	1	µs
	Fall time	T_F	38	SIM-IO = 30 pF	—	—	1	µs

■ TYPICAL CHARACTERISTICS

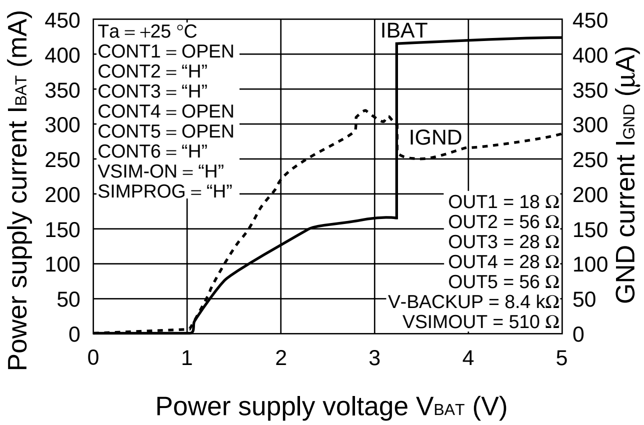
Power supply current vs. power supply voltage



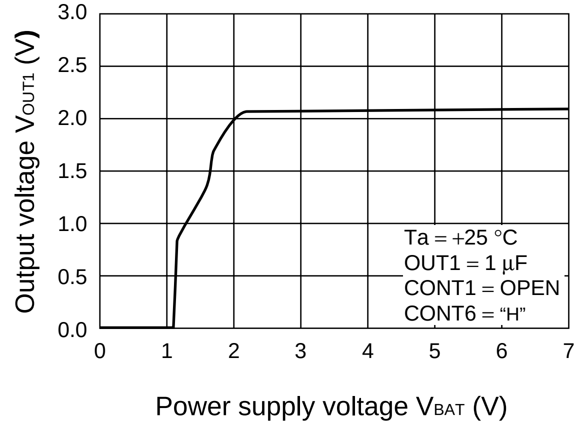
Power supply current vs. power supply voltage



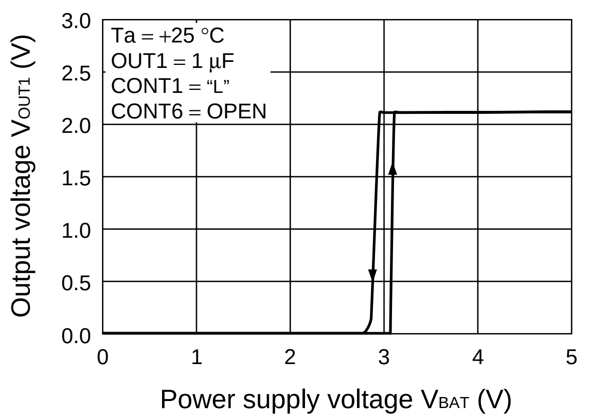
Power supply current , GND current vs. power supply voltage



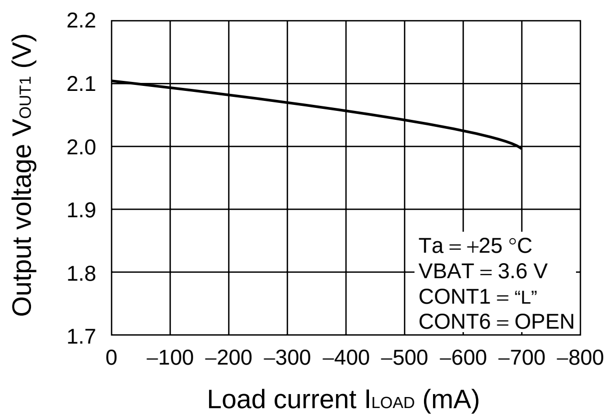
Output voltage vs. power supply voltage (LDO1)



Output voltage vs. power supply voltage (LDO1)

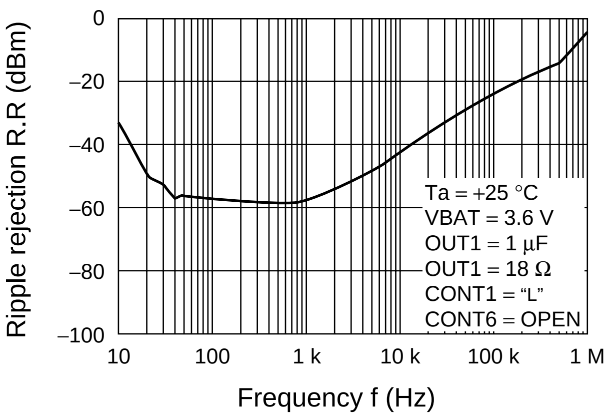


Output voltage vs. load current (LDO1)

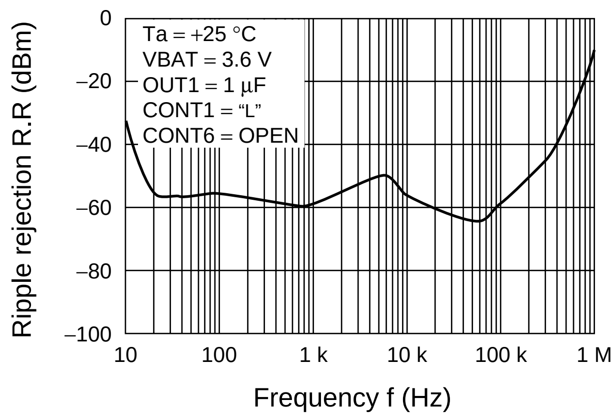


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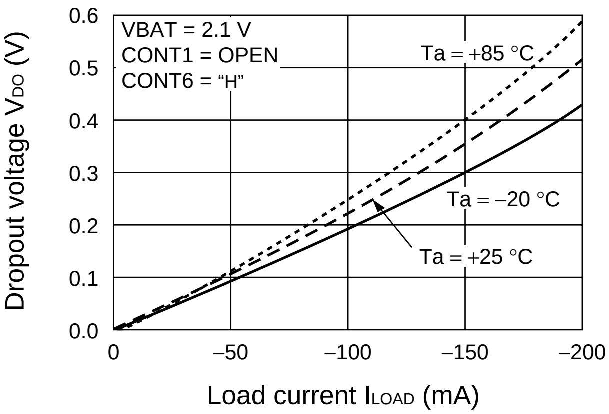
Ripple rejection vs. frequency (LDO1)



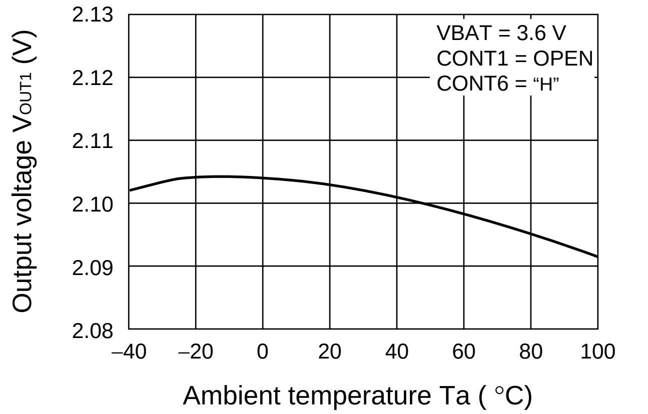
Ripple rejection vs. frequency (LDO1)



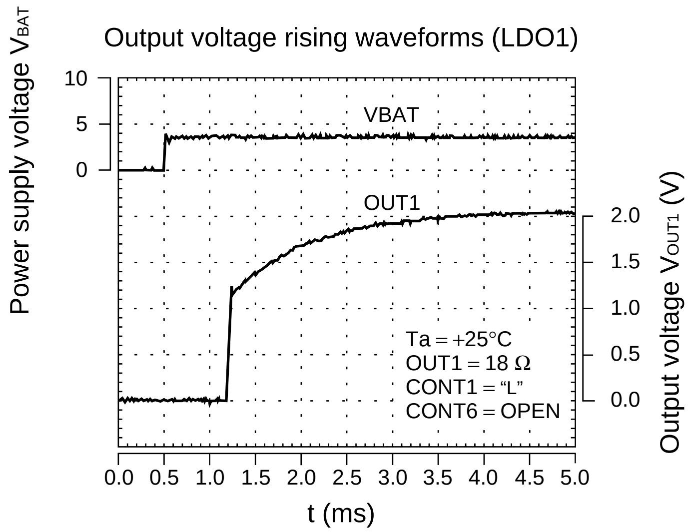
Dropout voltage vs. load current (LDO1)



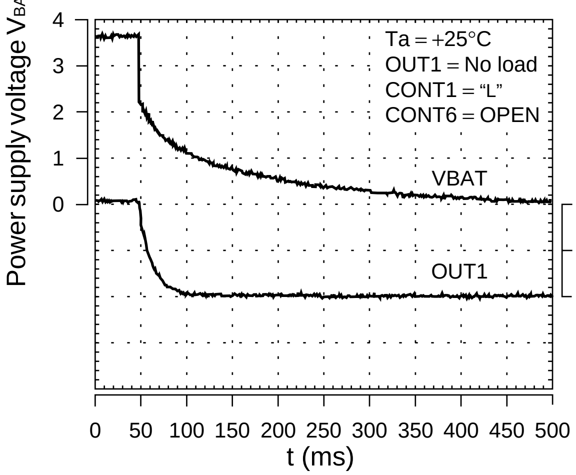
Output voltage vs. ambient temperature (LDO1)



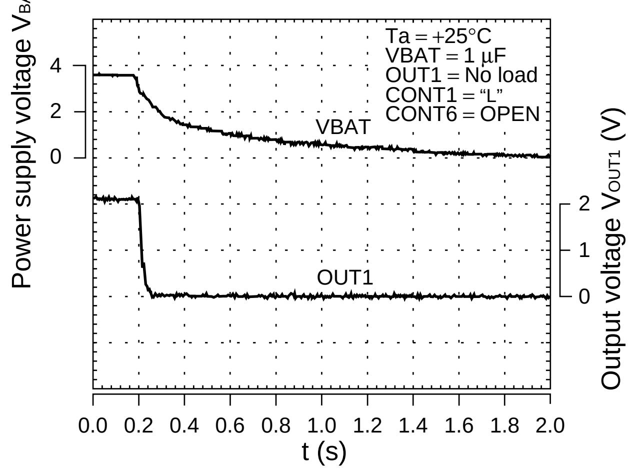
Output voltage rising waveforms (LDO1)



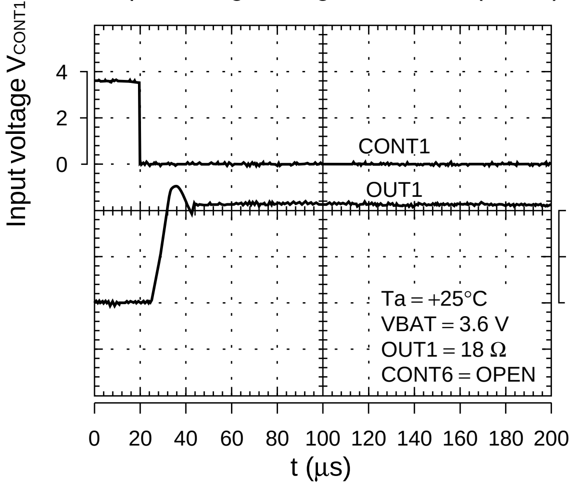
Output voltage falling waveforms (LDO1)



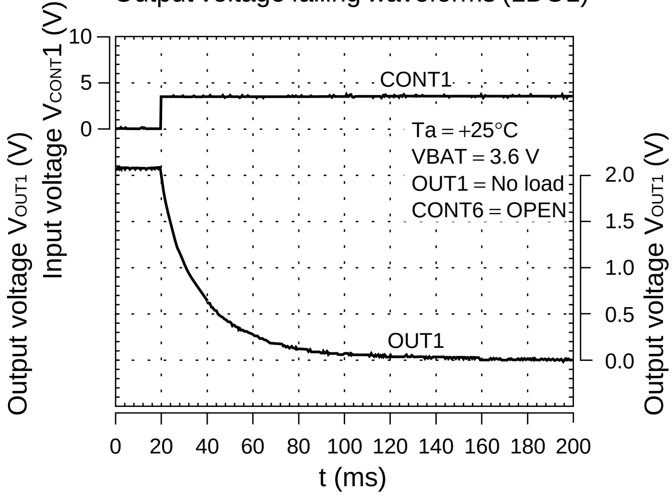
Output voltage falling waveforms (LDO1)



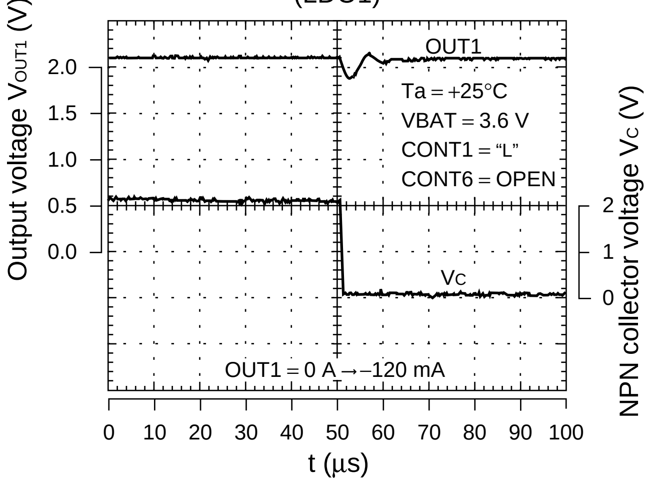
Output voltage rising waveforms (LDO1)



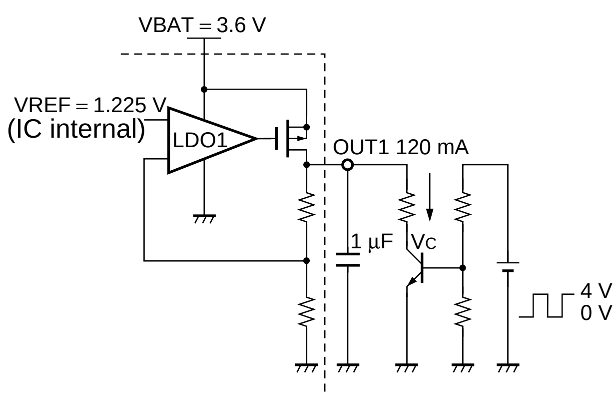
Output voltage falling waveforms (LDO1)



Waveform at rapid change of output load (LDO1)

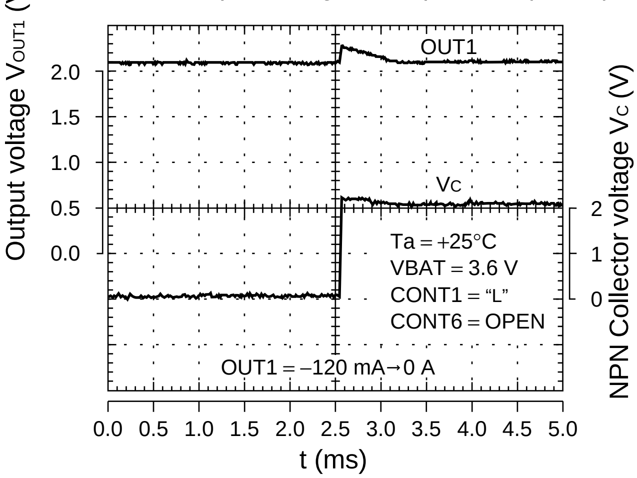


[Measurement diagram]

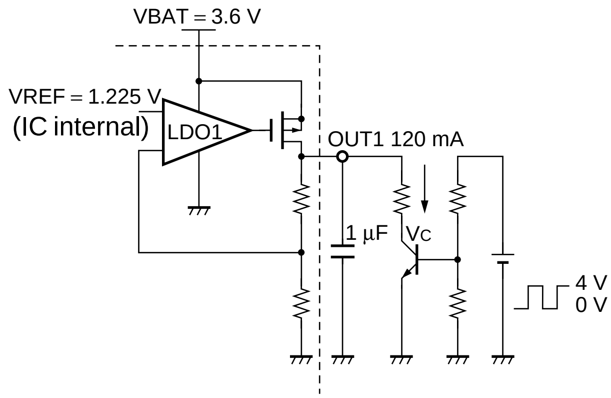


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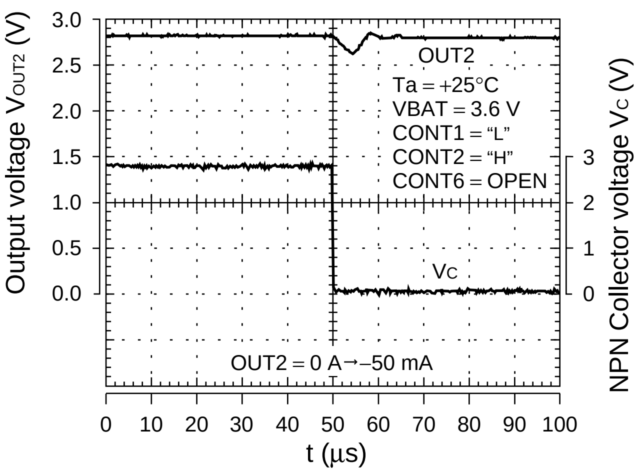
Waveform at rapid change of output load (LDO1)



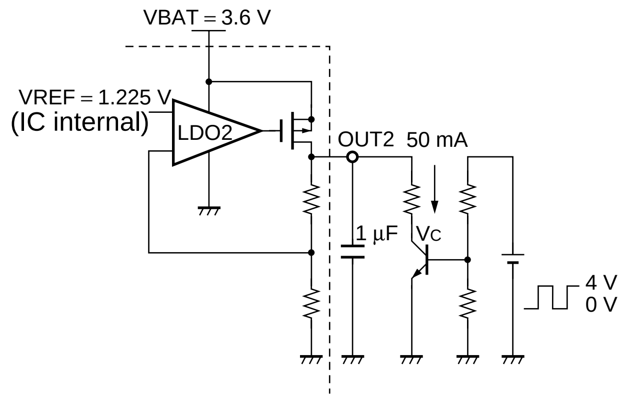
[Measurement diagram]



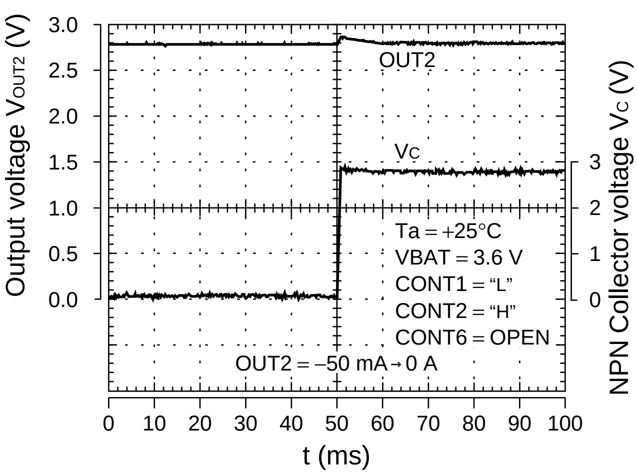
Waveform at rapid change of output load (LDO2)



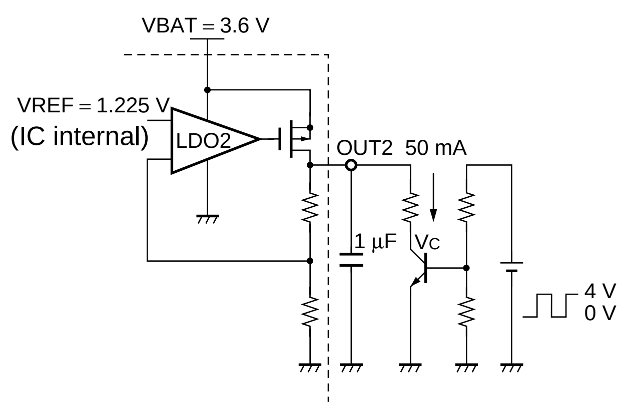
[Measurement diagram]



Waveform at rapid change of output load (LDO2)

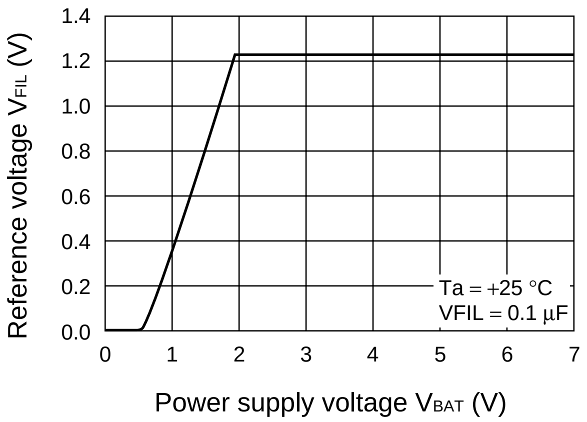


[Measurement diagram]

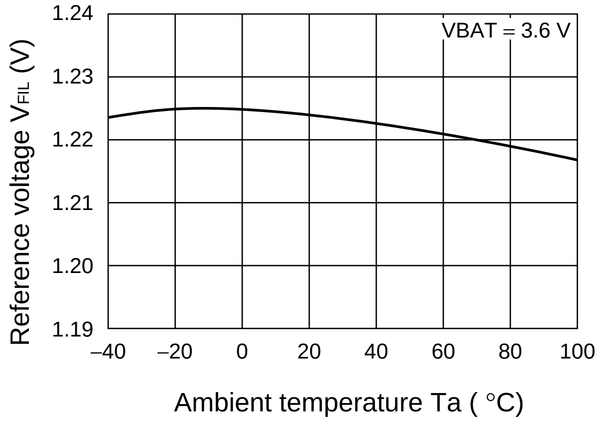


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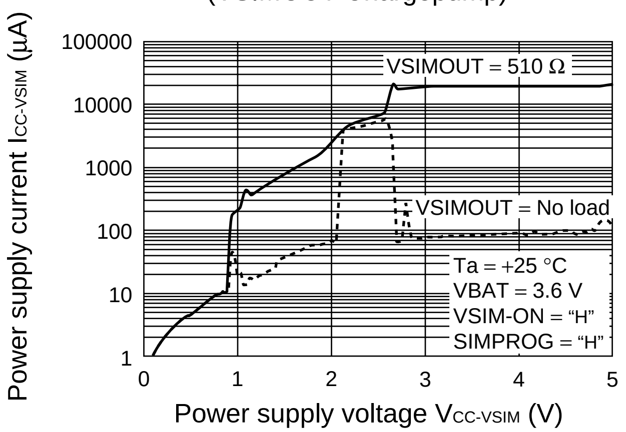
Reference voltage vs. power supply voltage



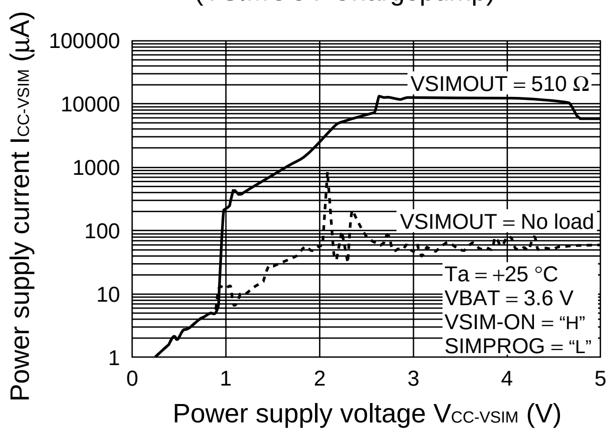
Reference voltage vs. ambient temperature



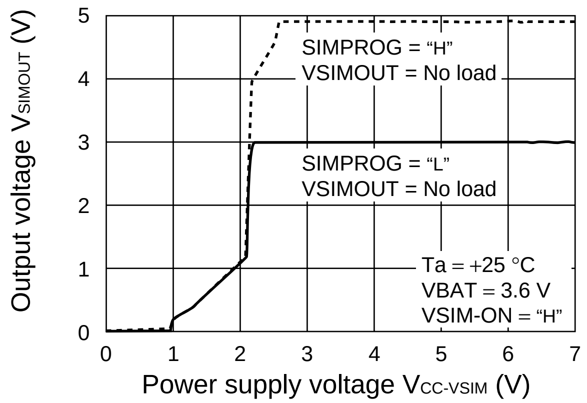
Power supply current vs. power supply voltage (VSIMOUT Chargepump)



Power supply current vs. power supply voltage (VSIMOUT Chargepump)

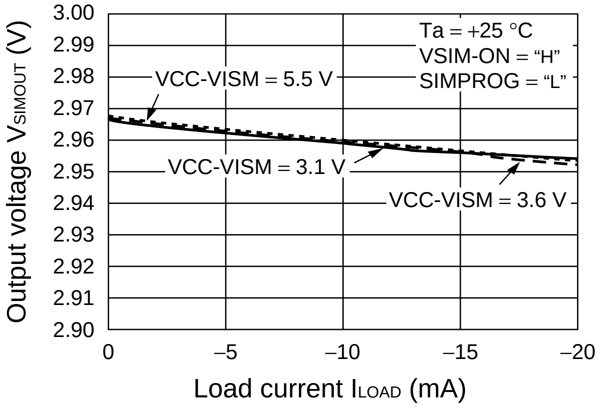


Output voltage vs. power supply voltage (VSIMOUT Chargepump)

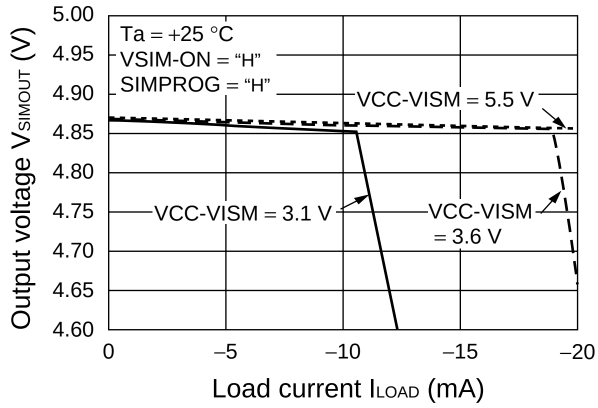


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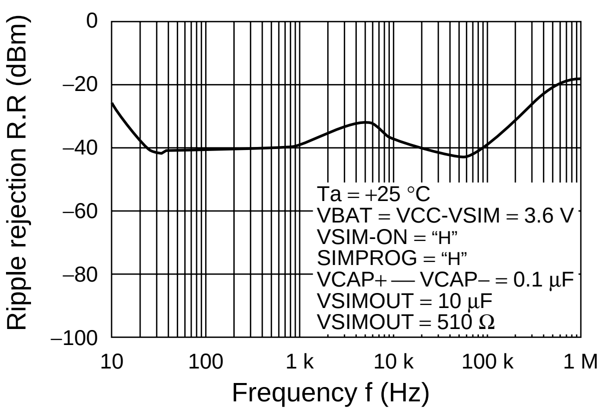
Output voltage vs. load current
(VSIMOUT Chargepump)



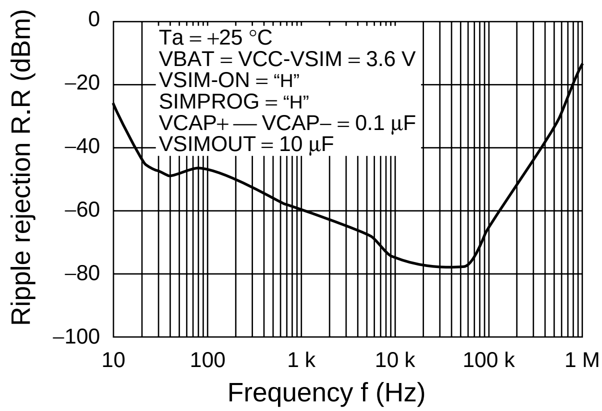
Output voltage vs. load current
(VSIMOUT Chargepump)



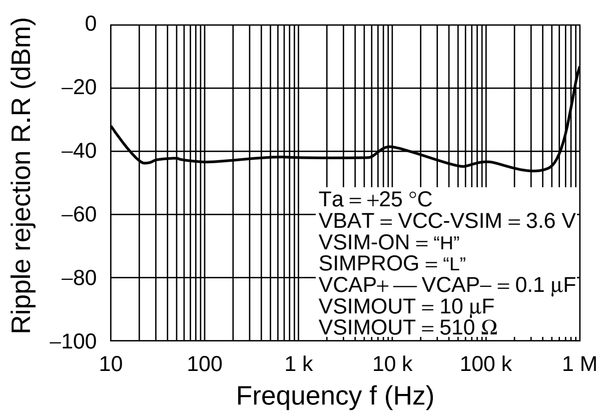
Ripple rejection vs. frequency
(VSIMOUT Chargepump)



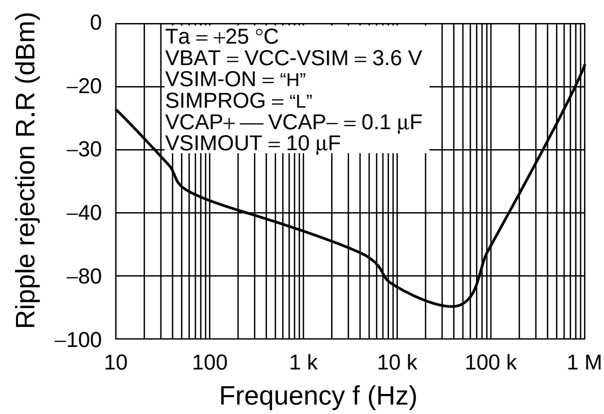
Ripple rejection vs. frequency
(VSIMOUT Chargepump)



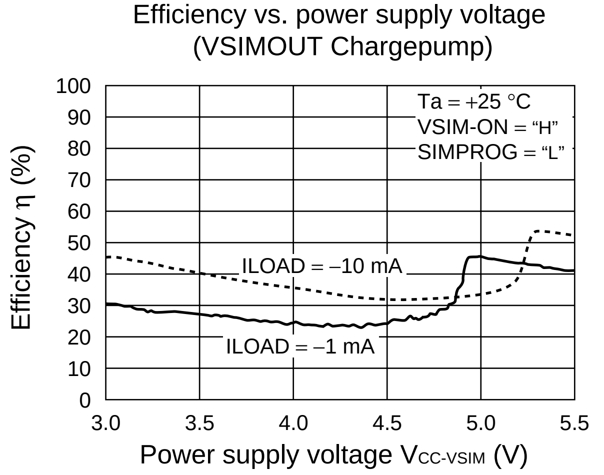
Ripple rejection vs. frequency
(VSIMOUT Chargepump)

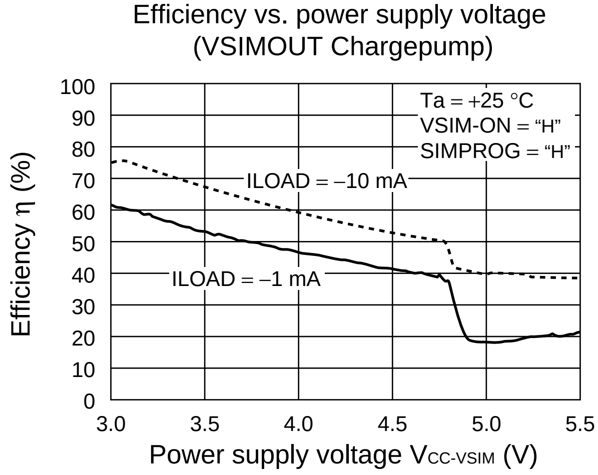


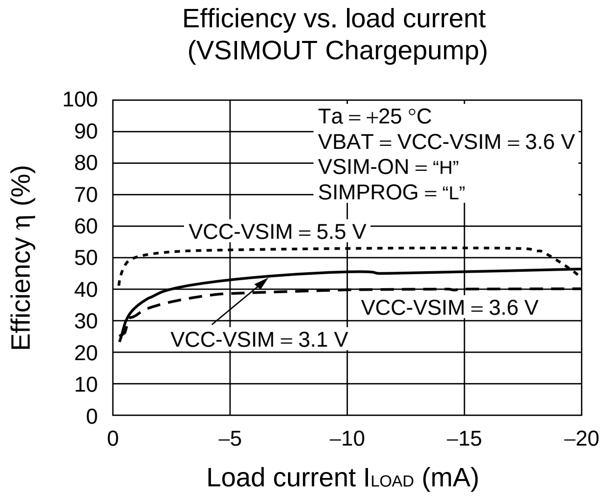
Ripple rejection vs. frequency
(VSIMOUT Chargepump)

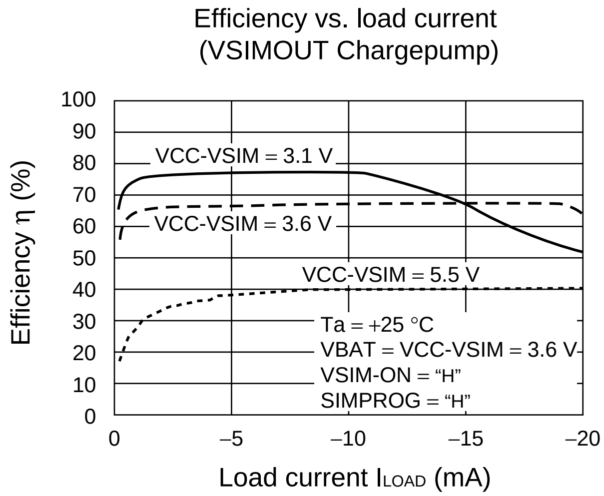


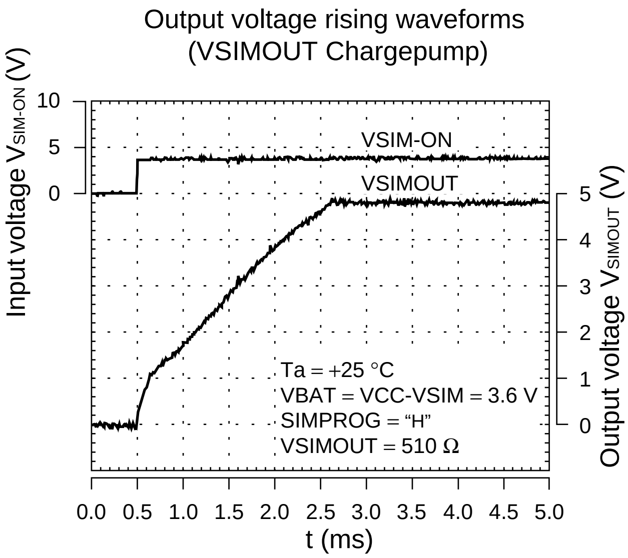
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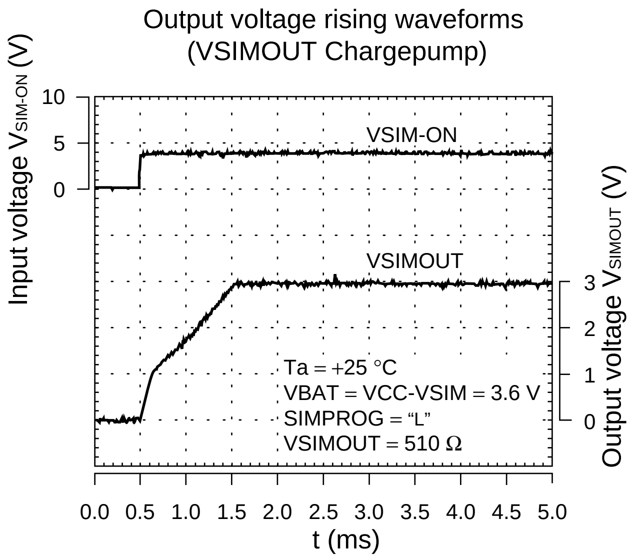

Efficiency vs. power supply voltage
(VSIMOUT Chargepump)
Ta = +25 °C
VSIM-ON = "H"
SIMPROG = "L"
ILOAD = –10 mA
ILOAD = –1 mA
Efficiency η (%)
Power supply voltage VCC-VSIM (V)


Efficiency vs. power supply voltage
(VSIMOUT Chargepump)
Ta = +25 °C
VSIM-ON = "H"
SIMPROG = "H"
ILOAD = –10 mA
ILOAD = –1 mA
Efficiency η (%)
Power supply voltage VCC-VSIM (V)


Efficiency vs. load current
(VSIMOUT Chargepump)
Ta = +25 °C
VBAT = VCC-VSIM = 3.6 V
VSIM-ON = "H"
SIMPROG = "L"
VCC-VSIM = 5.5 V
VCC-VSIM = 3.6 V
VCC-VSIM = 3.1 V
Efficiency η (%)
Load current ILOAD (mA)

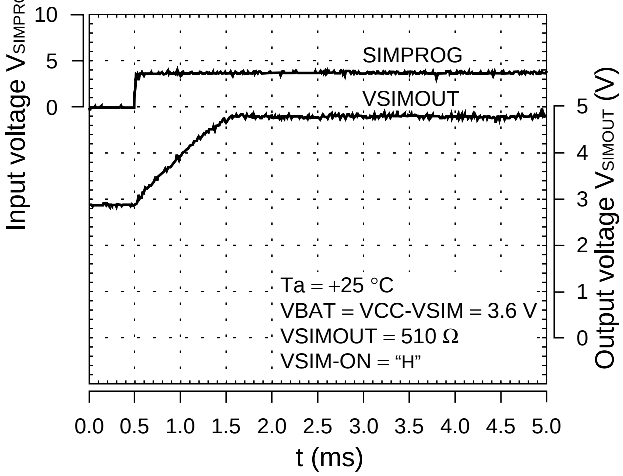

Efficiency vs. load current
(VSIMOUT Chargepump)
VCC-VSIM = 3.1 V
VCC-VSIM = 3.6 V
VCC-VSIM = 5.5 V
Ta = +25 °C
VBAT = VCC-VSIM = 3.6 V
VSIM-ON = "H"
SIMPROG = "H"
Efficiency η (%)
Load current ILOAD (mA)


Output voltage rising waveforms
(VSIMOUT Chargepump)
VSIM-ON
VSIMOUT
Ta = +25 °C
VBAT = VCC-VSIM = 3.6 V
SIMPROG = "H"
VSIMOUT = 510 Ω
Input voltage VSIM-ON (V)
Output voltage VSIMOUT (V)
t (ms)

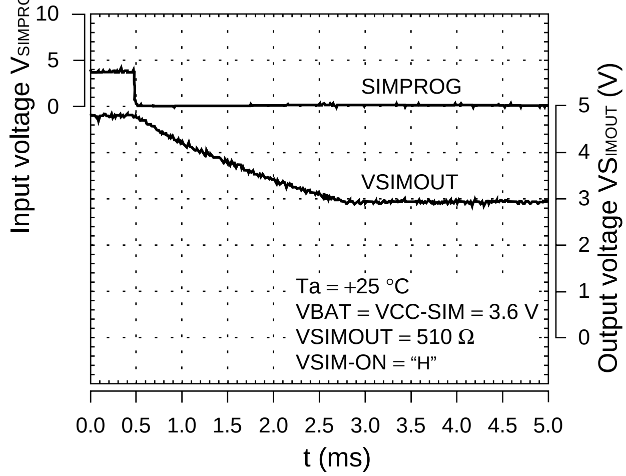

Output voltage rising waveforms
(VSIMOUT Chargepump)
VSIM-ON
VSIMOUT
Ta = +25 °C
VBAT = VCC-VSIM = 3.6 V
SIMPROG = "L"
VSIMOUT = 510 Ω
Input voltage VSIM-ON (V)
Output voltage VSIMOUT (V)
t (ms)

(Continued)

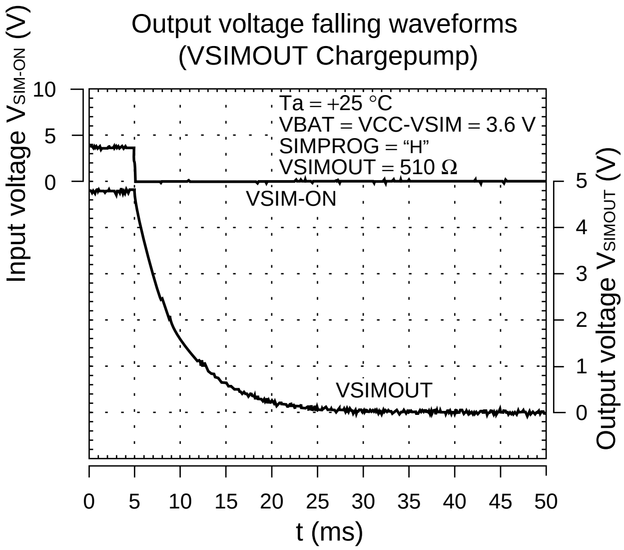
Output voltage rising waveforms
(VSIMOUT Chargepump)



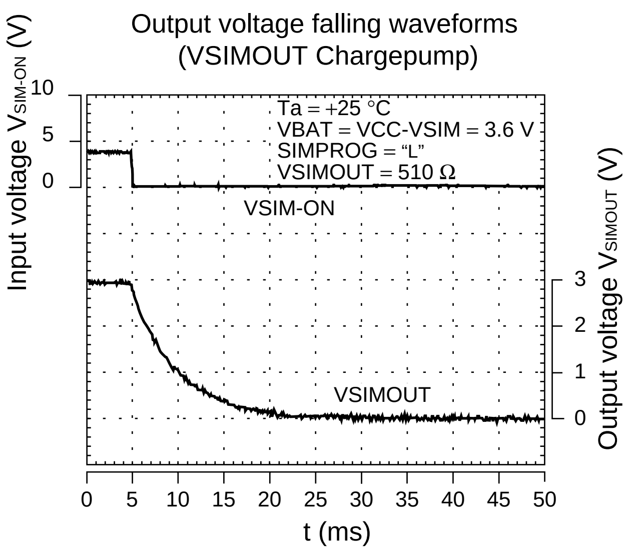
Output voltage falling waveforms
(VSIMOUT Chargepump)



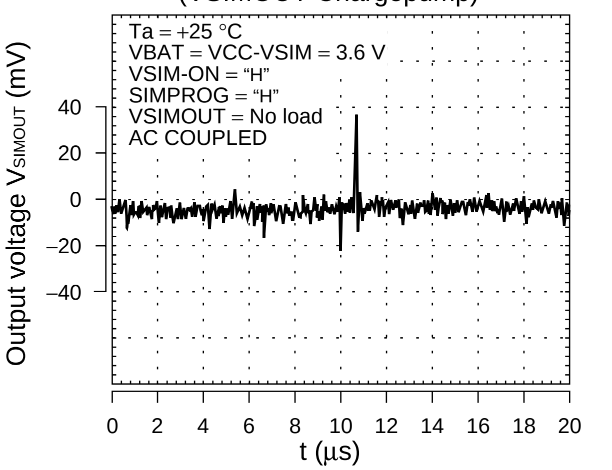
Output voltage falling waveforms
(VSIMOUT Chargepump)



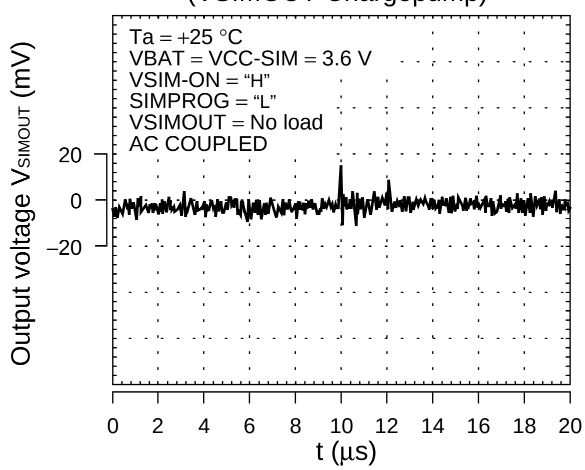
Output voltage falling waveforms
(VSIMOUT Chargepump)



Output voltage waveforms
(VSIMOUT Chargepump)

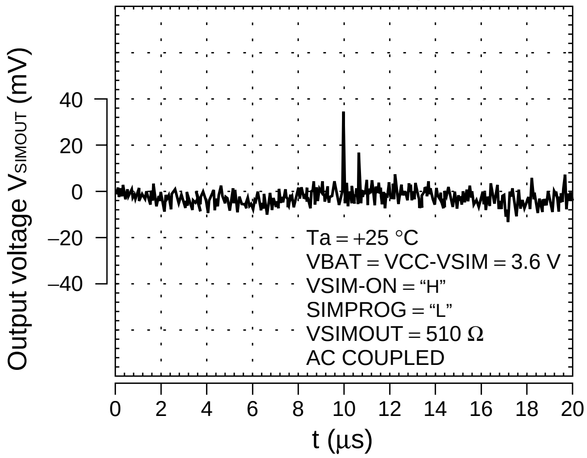


Output voltage waveforms
(VSIMOUT Chargepump)

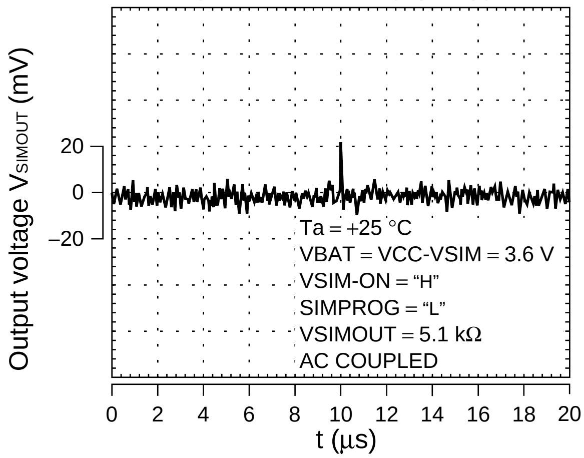


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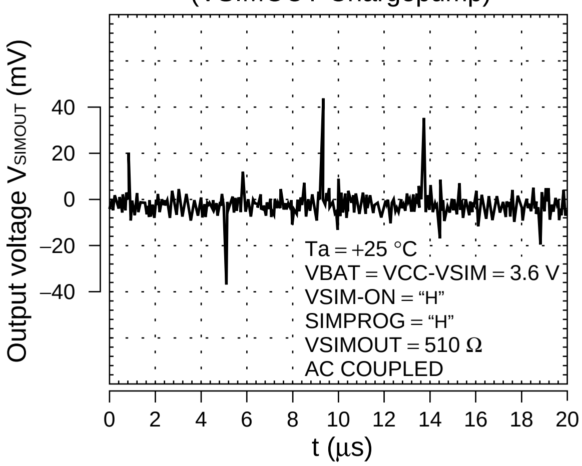
Output voltage waveforms
(VSIMOUT Chargepump)



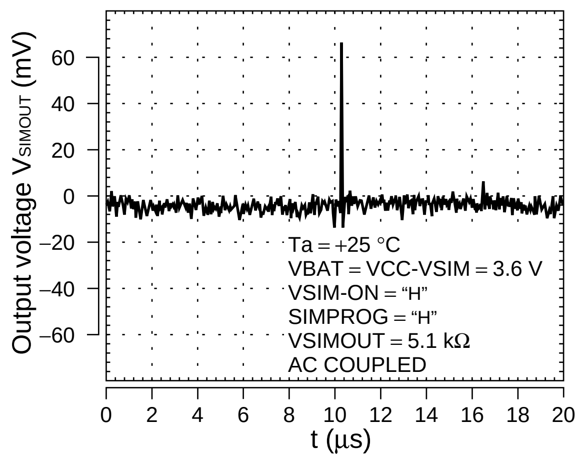
Output voltage waveforms
(VSIMOUT Chargepump)



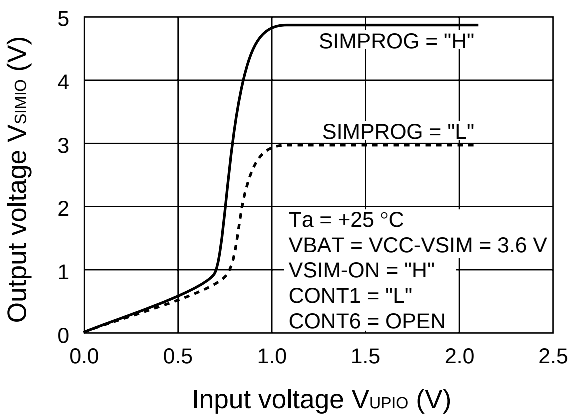
Output voltage waveforms
(VSIMOUT Chargepump)



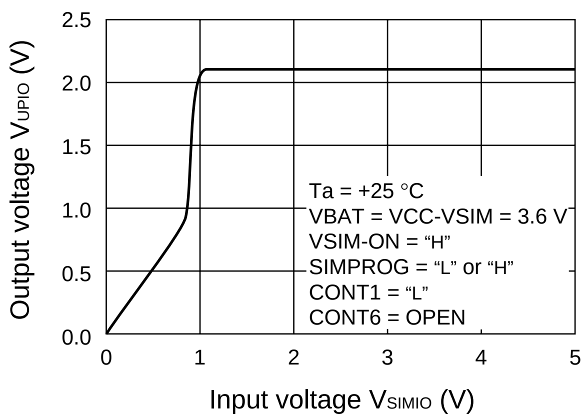
Output voltage waveforms
(VSIMOUT Chargepump)



Output voltage vs. input voltage (SIM Inter-



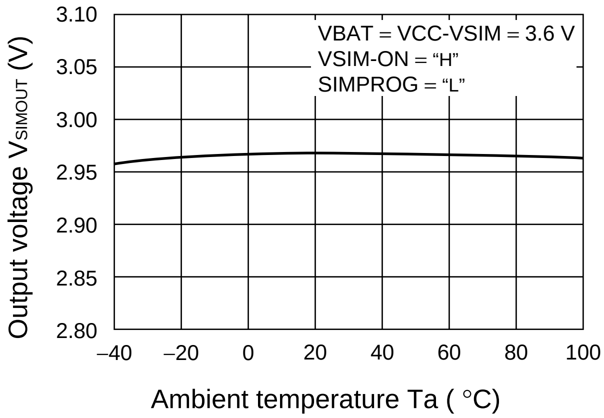
Output voltage vs. input voltage (SIM Interface)



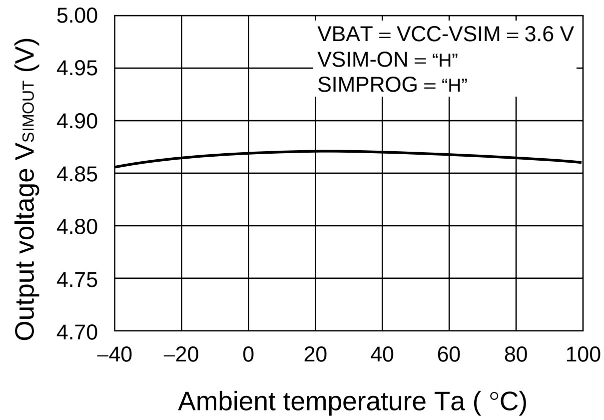
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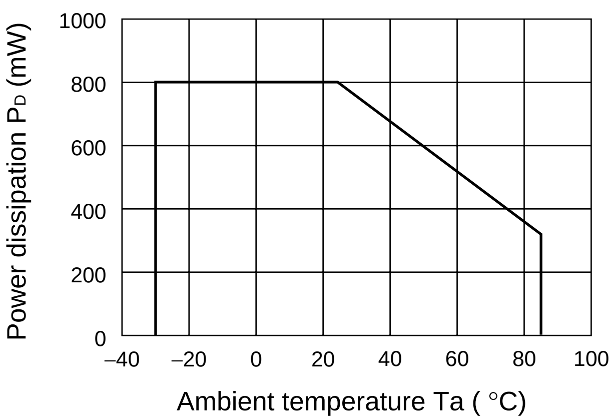
Output voltage vs. ambient temperature (SIM Interface)



Output voltage vs. ambient temperature (SIM Interface)



Power dissipation vs. ambient temperature



■ FUNCTIONAL DESCRIPTION

(1) MAIN UVLO/BACKUP UVLO

Transient power-on surge states or sudden drops in supply voltage (VBAT2) can cause an IC to operate abnormally, leading to destruction or damage to system elements. To prevent this type of fault, the undervoltage lockout circuits (UVLO/ Backup UVLO) will shut off the output from OUT1 to V-BACKUP if the supply voltage falls below the UVLO circuit threshold voltage (3.0 V/2.8 V typ.). System operation is restored as soon as the supply voltage rises above the UVLO circuits threshold voltage (3.2 V typ.).

(2) LDO1

The LDO1 circuits uses the reference voltage supply and generates an output voltage (2.1 V typ.) at the OUT1 terminal (pin 12,13). Power can be drawn from the OUT1 terminal for external use, up to a maximum load current of 120 mA.

(3) XPOWERGOOD (RESET)

When the OUT1 terminal (pin 12,13) voltage exceeds 2.0 V (typ.), after a delay interval set by a capacitor ($C_{DELAYCAP}$) connected to the DELAYCAP terminal (pin 18), the XPOWERGOOD terminal (pin 17) goes to “H” level and resets the microcomputer. At the same time, the LDO2, LDO3, and LDO4 output is controlled ON/OFF.

(4) LDO2

The LDO2 circuit uses the reference voltage supply and generates an output voltage (2.8 V typ.) at the OUT2 terminal (pin 6,7) when the XPOWERGOOD terminal (pin 17) voltage is at “H” level and an “H” level signal is input at the CONT2 terminal (pin 16). Power can be drawn from the OUT2 terminal for external use, up to a maximum load current of 50 mA.

(5) General Purpose switches

Any of the OUT terminals can be connected to any SW-INPUT terminal so that when the corresponding SW-ON terminal is at “H” level, the OUT terminal voltage can be drawn from the associated SW-OUTPUT terminal.

(6) LDO3

The LDO3 circuits uses the reference voltage supply and generates an output voltage (2.8 V typ.) at the OUT3 terminal (pin 3,4) when the XPOWERGOOD terminal (pin 17) voltage is at “H” level and an “H” level signal is input at the CONT3 terminal (pin 56). Power can be drawn from the OUT3 terminal for external use, up to a maximum load current of 100 mA.

(7) LDO4

The LDO4 circuits uses the reference voltage supply and generates an output voltage (2.8 V typ.) at the OUT4 terminal (pin 40,41) when the XPOWERGOOD terminal (pin 17) voltage is at “H” level and an “H” level signal is input at the CONT3 terminal (pin 56) , and an “L” level signal is input at the CONT4 terminal (pin 44). When an “H” level signal is input at the CONT4 terminal, the output voltage at the OUT4 terminal is 2.5 V (typ.). Power can be drawn from the OUT4 terminal for external use, up to a maximum load current of 100 mA.

(8) LDO5

The LDO5 circuits uses the reference voltage supply and generates an output voltage (2.8 V typ.) at the OUT5 terminal (pin 57) when the OUT1 terminal (pin 12,13) is in output state and an “H” level signal is input at the CONT5 terminal (pin 57). Power can be drawn from the OUT5 terminal for external use, up to a maximum load current of 50 mA.

(9) LDO6

The LDO6 circuit uses the reference voltage supply and generates an output voltage (2.1 V typ.) at the V-BACKUP terminal (pin 21). Power can be drawn for external use, from the V-BACKUP terminal, up to a maximum load current of 250 µA.

(10) REF-OUT

This circuit uses the reference voltage generated by the reference voltage block (1.225 V typ.) to produce a temperature compensated reference voltage (1.225 V typ.) at the REF-OUT terminal(pin 24) by means of a voltage follower. The reference voltage can also be drawn from the REF-OUT terminal for external use, up to a load current of 50 µA.

(11) VSIMOUT Chargepump

The VSIMOUT charge pump uses the voltage from the battery and generates 5.0 V (typ.) voltage at the VSIMOUT terminal (pin 29) when an “H” level signal is input at the SIMPROG terminal (pin 27) , or 3.0 V (typ.) voltage when an “L” level signal input at the SIMPROG terminal. This voltage can also be drawn from the VSIMOUT terminal for external use, up to a load current of 10 mA.

(12) GSM/SIM Logic Translation µP Interface

When a signal is input from the microprocessor to the RESET-IN terminal(pin 33) and CLK-IN terminal (pin 34), a level-shifted voltage is output from the RST terminal (pin 36) and CLK terminal (pin 37) to the SIM card. The µP-IO terminal (pin 35) and SIM-IO terminal (pin 38) are input/output pins and carry signals between the microprocessor and SIM card.

(13) SIM Interface 5 V (SIMPROG = “H”)

When an “H” level signal is input to the SIMPROG terminal (pin 27), 5.0 V (typ.) voltage is generated from the VSIMOUT terminal (pin 29) as a power supply for the SIM card.

(14) SIM Interface 3 V (SIMPROG = “L”)

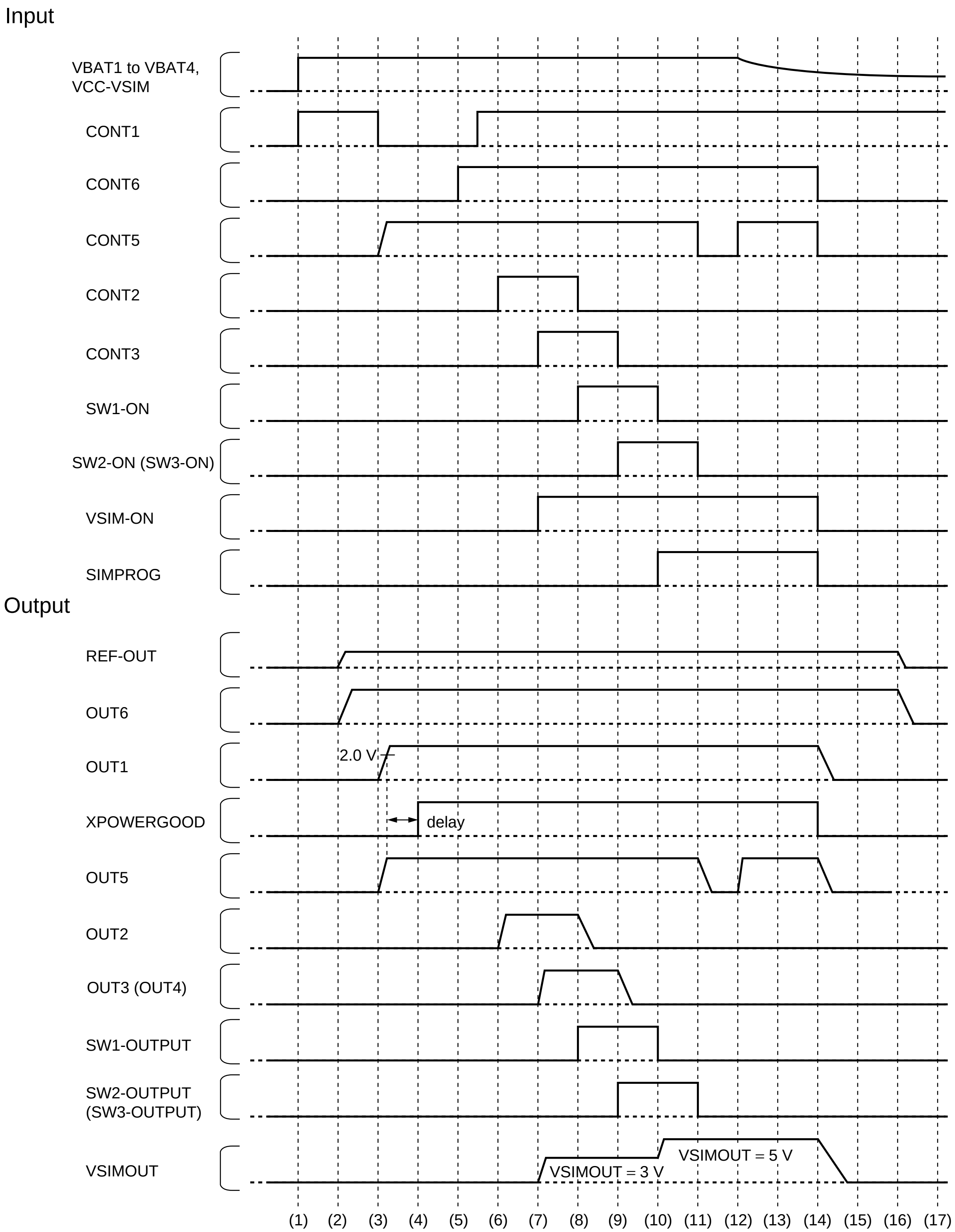
When an “L” level signal is input to the SIMPROG terminal (pin 27), 3.0 V (typ.) voltage is generated from the VSIMOUT terminal (pin 29) as a power supply for the SIM card.

■ SETTING THE XPOWERGOOD TIME

When the OUT1 terminal (pin 12,13) voltage exceeds 2.0 V (typ.), the capacitor ($C_{DELAYCAP}$) connected to the DELAYCAP terminal (pin 18) starts charging, the XPOWERGOOD terminal (pin 17) voltage rises. The XPOWERGOOD terminal voltage rising time (XPOWERGOOD time) can be set by a capacitor connected to the DELAYCAP terminal.

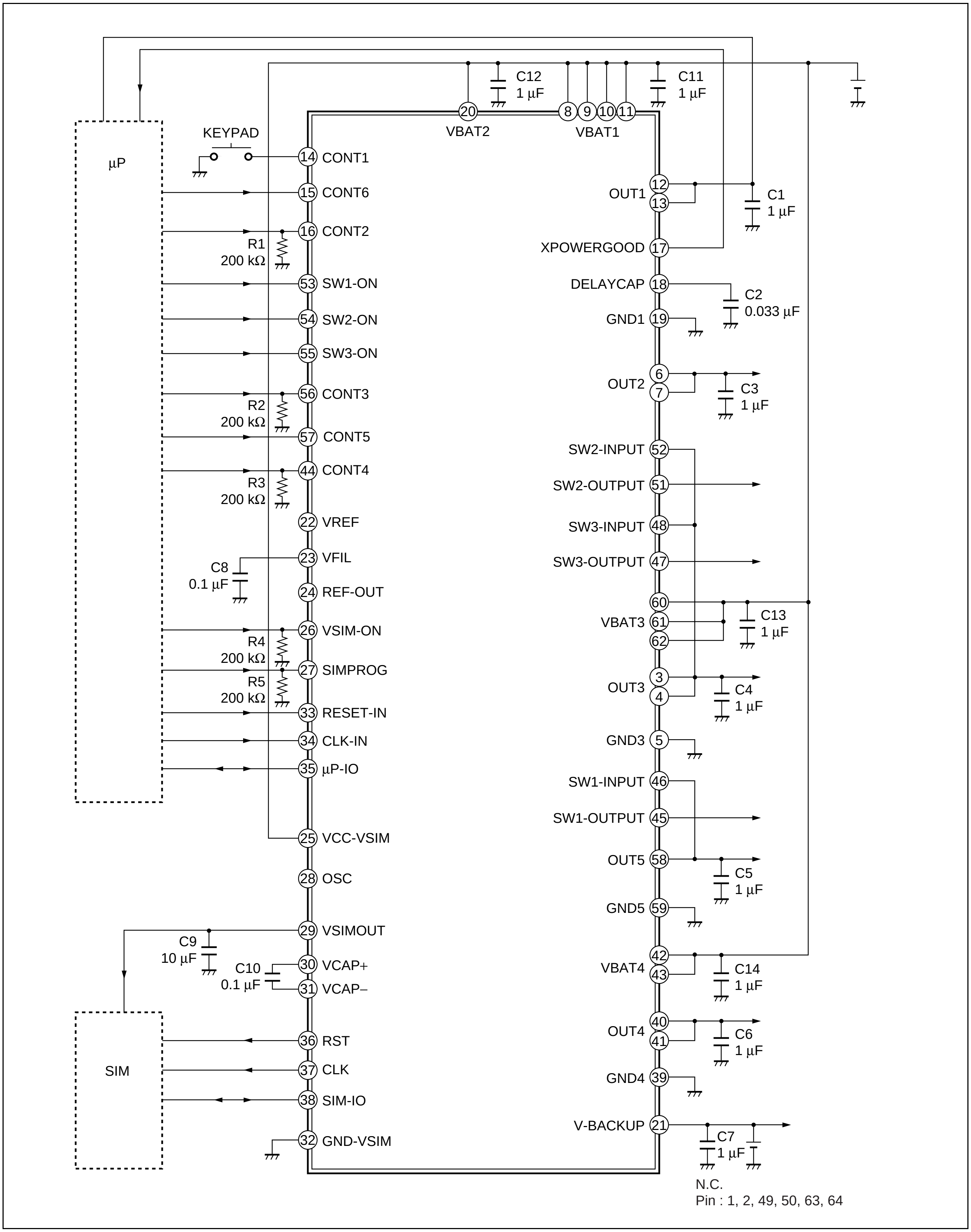
XPOWERGOOD time : T_{XPG} (s) $\fallingdotseq 0.8 \times C_{DELAYCAP}$ (µF)

■ OPERATION TIMING CHART



(1) : Battery controlled
(2) : BACKUP UVLO ON
(3) : phone turned on
(4) : XPOWERGOOD on
(5) : OUT1 hold
(6) to (12) : µP controlled
(14) : Main UVLO off
(16) : BACKUP UVLO off

■ APPLICATION EXAMPLE



■ USAGE PRECAUTIONS

• Printed circuit board ground lines should be set up with consideration for common impedance.

• Take appropriate static electricity measures.

- Containers for semiconductor materials should have anti-static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or Containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personal should be grounded with resistance of 250 kΩ to 1 MΩ between body and ground.

• Do not apply negative voltages

The use of negative voltages below -0.3V may create parasitic transistors on LSI lines, Which can cause abnormal operation.

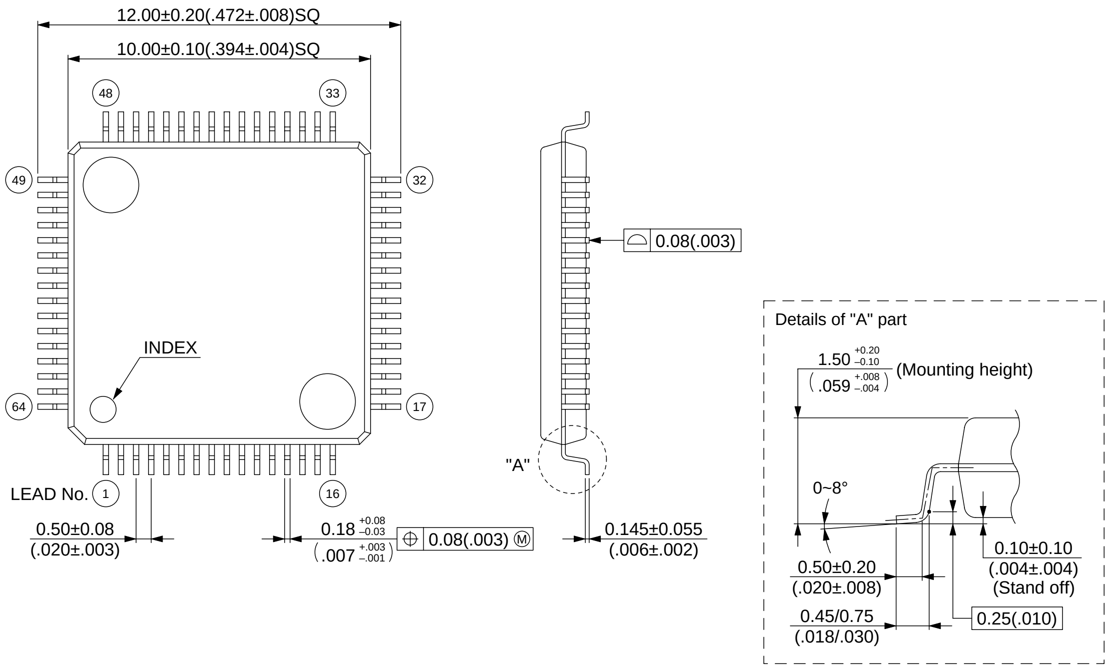
■ ORDERING INFORMATION

Part number	Package	Remarks
MB3891PFV	64-pin Plastic LQFP (FPT-64P-M03)	

■ PACKAGE DIMENSION

64-pin plastic LQFP
(FPT-64P-M03)

Note : Pins width and pins thickness include plating thickness.



Dimensions in mm (inches) .

FUJITSU LIMITED

F0007